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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/788,596	02/21/2001	Hirokazu Miyazaki	PA-1136	8771

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EXAMINER
PAREKH, NITIN

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 02/27/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/788,596	MIYAZAKI, HIROKAZU	
	Examiner	Art Unit	
	Nitin Parekh	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 November 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,12-14 and 17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,12-14 and 17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claim 14 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim 14, lines 2-5 cite: ".....each of said leads is connected to a corresponding one of a plurality of solder balls of said semiconductor chip, and said other end of each of said leads is connected to a corresponding one of a plurality of connection pads of said wiring substrate".

The above claim elements relate to the final mounting structure as described in Figures 1, 4a-4d and 6 showing the connections of the insulating sheet, chip and wiring substrate.

However, the independent claim 12, line 6 cites: "... other end of leads being shaped to be afloat in said holes", which relates to interim assembly/process steps as described in the specification and in Fig. 2 (see page 7, line 23- page 10, line 13) where

the leads are in a floating state and the insulating sheet, chip and wiring substrate are separated from each other.

Therefore, there is no support for the device comprising the leads being shaped afloat and being connected as recited in claim 14.

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 17 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01.

Claim 17, lines 2-6 cite: "a semiconductor chip which is provided with a plurality of solder balls, a wiring substrate which is provided with a plurality of connection pads; and an insulating sheet to be positioned……".

The structural relationship between the chip, the insulating sheet and the wiring substrate and their respective connection is not clear as cited in the claim language.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 12 and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Kitahara (US Pat. 5440452).

Regarding claim 12, Kitahara discloses an insulating tape/sheet (4 in Fig. 16) provided between a semiconductor chip and a wiring substrate (1 and 7 respectively in Fig. 16) comprising:

- a plurality of holes/windows (44 Fig. 1) there through
- a plurality of leads (3 in Fig. 1 and 16) on a first surface of the tape, the leads having two ends including a fixed end (left portion 3/31 of the lead on right side of the chip in Fig. 16) and an other end (right portion 32/33 of the lead on right side of the chip in Fig. 16)
- the other end having a variety of shapes comprising a hanging shape or shaped to be afloat in the hole (32/33 in Fig. 2-3d; Col. 7, line 15, 65 and Col. 8, line 25) and being protruded from the second surface of the insulating sheet (32 in Fig. 2-3c; Col. 5, line 50), and

- the plurality of connection bumps (11 in Fig. 2) being electrically connected through the fixed end and the other end of the lead to corresponding connection pads on the wiring substrate/board (Fig. 17; Col. 6, line 37)

(Fig. 16, 17 and 1-3d; Col. 5, line 20- Col. 6, line 60; Col. 7 and 8).

Regarding claim 13, as explained above for claim 12, Kitahara discloses the other end of the lead being protruded from the second surface through the hole (32 in Fig. 2-3c; Col. 5, line 50).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-9 and 14 insofar in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Kitahara (US Pat. 5440452) in view of Miyazaki et al (US Pat. 6342726).

Regarding claim 1, Kitahara discloses a mounting structure of a semiconductor package comprising:

- a semiconductor chip (1 in Fig. 2) which is provided with a plurality of connection bumps (11 in Fig. 2)
- a wiring substrate/board (7 in Fig. 17) which is provided with a plurality of connection pads (74 in Fig. 17)
- an insulating/polyimide sheet/film (4 in Fig. 1 and 2) having a plurality of leads (3 in Fig. 1 and 2) being provided between the chip and the wiring substrate/board (Fig. 16 and 17),
- the leads having two ends including a fixed end (left portion 3/31 in Fig. 2 and 12) and an other end (right portion 32/33 in Fig. 2 and 12), and
- the plurality of connection bumps (11 in Fig. 2) being electrically connected through the fixed end and the other end of the lead to corresponding connection pads on the wiring substrate/board (Fig. 17; Col. 6, line 37)

(Fig. 1-3d, 16 and 17; Col. 5, line 20- Col. 6, line 60; Col. 7 and 8).

Kitahara fails to specify the connection bumps of the chip being solder balls.

Miyazaki et al teach using a semiconductor chip having connection bumps in a form of solder balls, stud bumps, etc. (43/45 in Fig. 44 and 47 respectively; Col. 21, line 50- Col. 22, line 45).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate a plurality of solder balls on the chip as taught by

Miyazaki et al so that the interconnect integrity and reliability can be improved in Kitahara's structure.

Regarding claim 2, Kitahara discloses the insulating sheet having holes (44 in Fig. 1 and 2) there through at positions corresponding to the connection pads (Fig. 17).

Regarding claim 3, Kitahara discloses one end of each of the leads being fixed on a first surface of the insulating sheet (31/3 in Fig. 2 and 12) and the other end having a variety of shapes comprising a hanging shape or shaped to be afloat in the hole (32/33 in Fig. 2-3d; Col. 7, line 15, 65 and Col. 8, line 25) and being protruded from the second surface of the insulating sheet (32 in Fig. 2-3c; Col. 5, line 50).

Regarding claim 4, as explained above for claim 3, Kitahara discloses the other end of the lead being protruded from the second surface through the hole (32/33 in Fig. 2-3c; Col. 5, line 50).

Regarding claim 5, as explained above for claim 1, Kitahara the connection bumps being electrically connected to the fixed end of the lead but fail to specify the specify the connection bumps of the chip being solder balls.

Miyazaki et al teach using a semiconductor chip having connection bumps in a form of solder balls, stud bumps, etc. (43/45 in Fig. 44 and 47 respectively; Col. 21, line 50- C0ol. 22, line 45).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate a plurality of solder balls on the chip being electrically connected to the fixed end of the lead as taught by Miyazaki et al so that the interconnect integrity and reliability can be improved in Kitahara's structure.

Regarding claim 6, as explained above for claims 1 and 4, Kitahara discloses each of the connection pads being electrically connected to the other end of respective leads.

Regarding claim 7, Kitahara discloses the leads being formed of conductive/resilient material such as copper or plated tin (Col. 6, line 1-15).

Regarding claim 8, Kitahara discloses the gap between the insulating sheet and the wiring substrate being filled with a sealing resin (2 in Fig. 17; Col. 1).

Regarding claim 9, as explained above for claim 1, Kitahara discloses the insulating sheet being made of polyimide resin or an epoxy resin (Col. 5, line 37).

Regarding claim 14, Kitahara discloses substantially the entire claimed structure as applied to claims 12 and 13 above, except the plurality of connection bumps on the chip being solder balls.

Miyazaki et al teach using a semiconductor chip having connection bumps in a form of solder balls, stud bumps, etc. (43/45 in Fig. 44 and 47 respectively; Col. 21, line 50- Col. 22, line 45).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate a plurality of solder balls on the chip being electrically connected to the fixed end of the lead as taught by Miyazaki et al so that the interconnect integrity and reliability can be improved in Kitahara's structure.

8. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Grabbe (US Pat. 5173055) in view of Miyazaki et al (US Pat. 6342726).

Regarding claim 17, Grabbe discloses in combination:

an electronic/semiconductor device/chip (48 in Fig. 9) which is provided with

- a plurality of connection pads (53 in Fig. 9)
- a wiring substrate/board (40 in Fig. 8) which is provided with a plurality of connection pads (47 in Fig. 8)
- an insulating/laminate sheet (26/32 in Fig. 4) to be positioned between the device/chip and wiring substrate/board, and
- the insulating/laminate sheet having a plurality of leads/fingers (18 in Fig. 4) for electrically connecting the respective connection pads of the chip and the wiring substrate/board (Fig. 9) and further comprising a plurality of holes (28 in Fig. 4) there through, one end of each of the leads/fingers being fixed on a

first surface of the insulating sheet (18 in Fig. 4) and the opposite end being shaped to be afloat/cantilevered in the holes

(Fig. 1-4, 8 and 9; Col. 2, line 10- Col. 3, line 45).

Grabbe fails to specify the connection pads of the electronic device/chip being solder balls.

Miyazaki et al teach using a semiconductor chip having connection bumps in a form of solder balls, stud bumps, etc. (43/45 in Fig. 44 and 47 respectively; Col. 21, line 50- Col. 22, line 45).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate a plurality of solder balls on the chip as taught by Miyazaki et al so that the interconnect integrity and reliability can be improved in Grabbe's structure.

Response to Arguments

10. Applicant's arguments with respect to claims 1-9, 12-14 and 17 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 703-305-3410. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722, 703-308-7724 or 703-872-9318 (Right FAX) for regular communications; 703-872-9310 (Right FAX) for After Final communications and 703-872-9310 (Right FAX) for customer service.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-3431.

Nitin Parekh

NP
02-23-03